a pMOSFET and an nMOSFET, wherein the channel of said pMOSFET and the channel of said nMOSFET are formed in said strained surface layer.

15. An integrated circuit comprising:

a heterostructure including a Si substrate, a relaxed $Si_{1-x}Ge_x$ layer on said Si substrate, and a strained surface layer on said relaxed $Si_{1-x}Ge_x$ layer, the heterostructure further including a planarized surface positioned between the strained surface layer and the Si substrate; and

a p-channel transistor and an n-channel transistor formed in said heterostructure, wherein said strained layer comprises the channel of said n-channel transistor and said p-channel transistor, and said n-channel transistor and said p-channel transistor are interconnected in a CMOS circuit.

Support for the amendments is found in claims 2 and 16, as originally filed. No new matter has been added. In accordance with 37 C.F.R. § 1.121 and the Notice published in the Official Gazette on February 25, 2003, attached is a listing of all pending claims submitted in a revised format.

REMARKS

Status of the Claims

Prior to entry of this Amendment and Response, claims 1-27 were pending. Claims 1 and 15 are independent claims.

- Claims 8, 10, and 15 are objected to because of alleged informalities.
- Claims 13 and 14 stand rejected under 35 U.S.C. §112, second paragraph, as allegedly indefinite.
- Claims 1, 2, 4, 6, 12, 15, 16, 18, 20, 26, and 27 stand rejected under 35 U.S.C. §102(e) as allegedly anticipated by U.S. Patent No. 5,998,807 to Lustig et al. ("Lustig").
- Claims 3, 7-11, 17, and 21 stand rejected under 35 U.S.C. §103(a) as allegedly unpatentable over Lustig.
- Claims 5 and 19 stand rejected under 35 U.S.C. §103(a) as allegedly unpatentable over Lustig in view of U.S. Patent No. 5,906,951 to Chu et al. ("Chu").
- Claims 13, 14, and 22-25 stand rejected under 35 U.S.C. §103(a) as allegedly unpatentable over Lustig in view of U.S. Patent No. 6,316,301 to Kant ("Kant").